IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Paton et al.

Title: OFFSET SPACER SMOS PROCESS FOR FORMING N-TYPE TRANSISTORS

Appl. No.: 10/619,877

Filing Date: 07/15/2003

Examiner: Christy L. Novacek

Art Unit: 2822

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

EV 505576442 US (Express Mail Label Number) 11/22/04 (Date of Deposit)

Roberta A. Cooper
(Printed Name)

Roberta A. Cooper
(Signature)

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

We, Eric N. Paton, Haihong Wang, and Qi Xiang, state and declare that:

1. Each of us is an inventor of at least one of Claims 1-20 currently pending in U.S. Patent Application No. 10/619,877 (hereinafter "the '877 application").

2. We understand that in an Office Action dated September 23, 2004, Claims 1-4, 7-10, and 17-20 were rejected as being unpatentable based in part on the use of U.S. Patent No. 6,762,085 to Zheng et al., entitled "METHOD OF FORMING A HIGH PERFORMANCE AND LOW COST CMOS DEVICE" (hereinafter "Zheng et al.").

3. We understand based on the information provided on the front page of Zheng et al. that Zheng et al. has a filing date of October 1, 2002.

4. At least by June 28, 2002, we conceived in the United States the ideas set forth in Claims 1-20 of the '877 application. Such conception is evidenced by the attached invention disclosure form pertaining to the subject matter of the present application, and which is dated June 28, 2002.

5. Based on the conception of the ideas set forth in Claims 1-20 at least by June 28, 2002, the subject matter recited in Claims 1-20 was invented by us prior to the October 1, 2002 filing date of Zheng et al.

6. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application or any patent issuing therefrom.

Date: 11/18/04 By: _____
Eric N. Paton

Date: 11/18/2004 By: _____
Haihong Wang

Date: 11/17/04 By: _____
Qi Xiang

Friday, June 28, 2002
SMOS Patent Harvesting Session, Group 4:
Technical Leader: Qi Xiang

I53, I89, I90 4-13

PRIORITY CODE
A____ B X
C____ D____

AMD INVENTION DISCLOSURE

TLD ID# 10970 Rec'd date _____

California & Asia: x42110, return to MS68; Texas: x55964 return to MS562; Dresden & Europe: x83401 Silke Kretzschmar at MS E21-PP.

This invention applies to: **Project:** ☐ **Product:** ☐ **Process:** ☐ **Technology:** ☐ **Other:** ☐

IMPORTANT Please identify any potential use: _____

List 2 to 5 key search words related to the invention: _____

Working title of invention: Offset spacer for NMOS As Extension implant to compensate for As enhanced diffusion

Inventor's signature : Eric Paton **date :** 6/28/02
Inventor's printed full name: _____ Citizenship: _____
Employee #: _____ Extension: _____ Mail stop: _____ Home telephone:( ) _____
AMD email address: _____ AMD office FAX:( ) _____
Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____
Residence address: _____
Post Office address: _____

Co-Inventor's signature : HaiHong Wang **date :** _____
Co-Inventor's printed full name: _____ Citizenship: _____
Employee #: _____ Extension: _____ Mail stop: _____ Home telephone:( ) _____
AMD email address: _____ AMD office FAX:( ) _____
Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____
Residence address: _____
Post Office address: _____

Co-Inventor's signature : Qi Xiang **date :** _____
Co-Inventor's printed full name: _____ Citizenship: _____
Employee #: _____ Extension: _____ Mail stop: _____ Home telephone:( ) _____
AMD email address: _____ AMD office FAX:( ) _____
Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____
Residence address: _____
Post Office address: _____

Co-Inventor's signature : _____ **date :** _____
Co-Inventor's printed full name: _____ Citizenship: _____
Employee #: _____ Extension: _____ Mail stop: _____ Home telephone:( ) _____
AMD email address: _____ AMD office FAX:( ) _____
Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____
Residence address: _____
Post Office address: _____

State total number of inventors here: ____. If there are more than four inventors, insert duplicate page 1.

HARVESTING LAW FIRM ATTORNEYS: FOLEY & LARDNER
Joe Ziebert, Ron Coslick
Witness 1 initial: _____ Witness 2 initial: _____

Patent Harvesting Breakout Session, Group 4: SMOS
Friday, June 28, 2002
Technical Leader: Qi Xiang

Participant Addresses
(Please verify all information and fill in any blank areas)

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Friday, June 28, 2002
SMOS Patent Harvesting Session, Group 4:
Technical Leader: Qi Xiang

AMD INVENTION DISCLOSURE

TLD ID# _____ Rec'd date _____

PRIORITY CODE
A____ B____
C____ D____

California & Asia: x42110, return to MS68; Texas: x55964 return to MS562; Dresden & Europe: x83401 Silke Kretzschmar at MS E21-PP.

Identify known relevant art (patents, publications, other information): _____

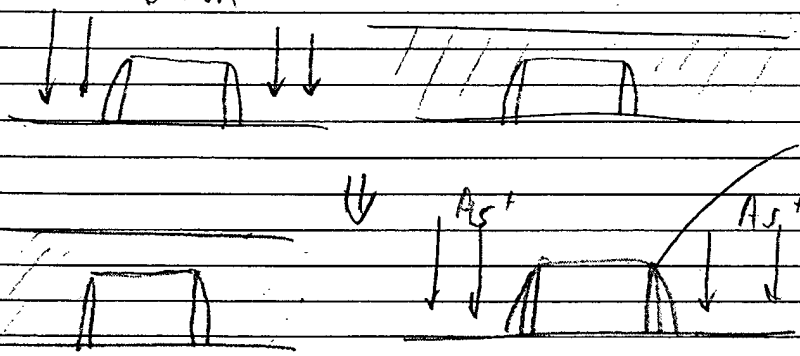
Offset spacer is used for Boron in current Si devices without SiGe. Offset spacer for Boron with be applied in this invention to Arsenic.

State the problem solved by the invention: _____

compensates for the enhanced lateral diffusion of Arsenic under the gate edge. To much overlap of the source/drain and the channel, will result in short channel effects.

Brief description and sketch of the invention (***please attach*** *copies of documents like AMD patent notebook pages, reports and drawings that are helpful in describing / understanding the invention*): _____

Surpressed Boron diffusion will prevent sufficient overlap of the gate and source/drain, resulting in too low of a drive current (Idsat)...



Patent notebook # _____ Page numbers _____ Number of drawings _____

HARVESTING LAW FIRM/ATTORNEYS: FOLEY & LARDNER
Joe Ziebert, Ron Coslick

Witness 1 initial: _____ Witness 2 initial: _____

Friday, June 28, 2002
SMOS Patent Harvesting Session, Group 4:
Technical Leader: Qi Xiang

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AMD INVENTION DISCLOSURE

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Advantages (check all that apply):

☐ simplifies manufacturing	☐ improves accuracy / precision	☐ reduces component parts
☐ reduces cost of manufacturing	☐ improves reliability	☐ improves signal to noise ratio
☐ improves density	☐ improves efficiency	☐ provides new functionality
☐ increases operating speed	☐ increases operating range	☐ other, explain below

Discussion of advantage(s) of the invention over other solutions
(*emphasize technical advance in the art* as measured against known art): the procedure is well established on current devices because Boron diffusal faster than Arsenic in Si devices.

Please *take special care to* ***preserve documentary evidence of the original date of conception of the invention.*** AMD Inventors' notebooks with witness signatures are useful in this regard. Notebooks are issued on request to inventors by the local AMD site Technical Librarian.

Please attach copy of first written description(s) of invention, with dates, names of persons with whom the description was discussed.
Please attach copy of first drawing(s) of invention, with date(s).

Describe any external disclosure of invention, place, date, circumstances of disclosure, with copy of NDA.

Does plan exist to publish, disclose or sell? No ☐, Yes ☐, If yes, where and when?_____

Was invention jointly developed with participation of inventors from outside AMD: No ☐, Yes ☐,
If yes, Company name_____,
If yes, name of AMD business contact and development contract no._____

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1
signature:_____Date:_____
Printed name:_____ Employee #:_____

Witness 2
signature:_____Date:_____
Printed name:_____ Employee #:_____

Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known: